WHAT IS CLAIMED IS:

1. A nonvolatile memory apparatus comprising:

a controller;

a plurality of terminals including a clock terminal, a command terminal and an other terminal;

a clock generator; and

a plurality of nonvolatile memory cells,

wherein said clock terminal is capable of receiving a first clock signal,

wherein said command terminal is capable of receiving commands which include a read command and a program command,

wherein said clock generator generates a second clock signal controlled by said controller,

wherein in an operation in response to said read command received from said command terminal, said nonvolatile memory apparatus is capable of reading data from ones of said nonvolatile memory cells, and outputs data to outside of said nonvolatile memory apparatus in response to said first clock signal via said other terminal except said command terminal,

wherein in an operation in response to said program command received from said command terminal, said, nonvolatile memory apparatus receives data from outside of said nonvolatile memory apparatus in response to said first clock signal via said other terminal except said command terminal and is capable of writing data to ones of said nonvolatile memory cells, and

wherein said data writing to ones of said nonvolatile memory cells is performed using said second clock signal.

2. A nonvolatile memory apparatus according to claim 1, wherein said operation in response to said program command includes a verify operation for verifying whether each of said nonvolatile memory cells completes writing data or not.

3. A nonvolatile memory apparatus according to claim 2, wherein each of said nonvolatile memory cells has a threshold voltage within an arbitrary one of a plurality of threshold voltage ranges,

wherein said threshold voltage ranges include a threshold voltage range indicating an erase state and a threshold voltage range indicating a program state,

wherein said nonvolatile memory apparatus controls moving said threshold voltage of one nonvolatile memory cell to within said threshold voltage range indicating said program state and staying said threshold voltages of remaining memory cells of ones of said nonvolatile memory cells within threshold voltage range indicating said erase state, in said operation in response to said program command.

4. A nonvolatile memory apparatus according to claim 3, wherein said commands further includes an erase command,

wherein in an operation in response to said erase command received from said command terminal, said nonvolatile memory apparatus erases data stored in ones of said nonvolatile memory cells, and

wherein said nonvolatile memory apparatus controls moving said threshold voltages of ones of said nonvolatile memory cells to within said

threshold voltage range indicating said erase state in said operation in response to said erase command.

5. A nonvolatile memory apparatus according to claim 4, further comprising;

a circuit,

wherein in said operation in response to said read command, said circuit senses a status of data according to threshold voltage of said nonvolatile memory cell which is within whether said threshold voltage range indicating said erase state or said threshold voltage range indicating said program state.

6. A nonvolatile memory apparatus according to claim 5, wherein said other terminal is a data terminal,

wherein said data terminal is capable of receiving data in said operation in response to said program command, and wherein said data terminal is capable of outputting data in said operation in response to said read command.

7. A nonvolatile memory apparatus according to claim 2, wherein each of said nonvolatile memory cells has a threshold voltage within an arbitrary one of a plurality of threshold voltage ranges,

wherein said threshold voltage ranges include a threshold voltage range indicating an erase state and a plurality of threshold voltage ranges each indicating a corresponding program state,

wherein said nonvolatile memory apparatus controls moving said threshold voltage of one nonvolatile memory cell to within one of said threshold voltage ranges indicating said program states according to data and staying said threshold voltages of remaining memory cells of ones of said nonvolatile memory cells, in said operation in response to said program command.

8. A nonvolatile memory apparatus according to claim 7, wherein said commands further include an erase command,

wherein in an operation in response to said erase command received from said command terminal, said nonvolatile memory apparatus erases data stored in ones of said nonvolatile memory cells, and

wherein said nonvolatile memory apparatus controls moving said threshold voltages of ones of said nonvolatile memory cells to within said threshold voltage range indicating said erase state in said operation in response to said erase command.

9. A nonvolatile memory apparatus comprising;

a controller;

a clock generator;

a clock terminal;

a data terminal;

a command terminal; and

a plurality of nonvolatile memory cells,

wherein said clock terminal is capable of receiving a first clock signal,

wherein said data terminal is capable of receiving data in response to said first clock signal and is capable of outputting data in response to said first clock signal,

wherein said command terminal is capable of receiving commands which include a read command and a program command,

wherein said clock generator generates a second clock signal controlled by said controller,

wherein in an operation in response to said read command received from said command terminal, said nonvolatile memory apparatus is capable of reading data from ones of said nonvolatile memory cells and serially outputs data to outside of said nonvolatile memory apparatus via said data terminal,

wherein in an operation in response to said program command received from said command terminal, said nonvolatile memory apparatus serially receives data from outside of said nonvolatile memory apparatus via said data terminal and is capable of writing data to ones of said nonvolatile memory cells, and

wherein said data writing to ones of said nonvolatile memory cells is performed using said second clock signal.

10. A nonvolatile memory apparatus according to claim 9, wherein said operation in response to said program command includes a verify operation for verifying whether each of ones nonvolatile memory cells completes writing data or not.

11. A nonvolatile memory apparatus according to claim 10, wherein

each of said nonvolatile memory cells has a threshold voltage within an arbitrary one of a plurality of threshold voltage ranges,

wherein said threshold voltage ranges include a threshold voltage range indicating an erase state and a threshold voltage range indicating a program state, and

wherein said nonvolatile memory apparatus controls moving said threshold voltage of one nonvolatile memory cell to within said threshold voltage range indicating said program state and staying said threshold voltages of remaining memory cells of ones of said nonvolatile memory cells within threshold voltage range indicating said erase state, in said operation in response to said program command.

12. A nonvolatile memory apparatus according to claim 11, wherein said commands further includes an erase command,

wherein in an operation in response to said erase command, said nonvolatile memory apparatus erases data stored in ones of said nonvolatile memory cells, and

wherein said nonvolatile memory apparatus controls moving said threshold voltages of ones of said nonvolatile memory cells to within said threshold voltage range indicating said erase state in said operation in response to said erase command.

13. A nonvolatile memory apparatus according to claim 12, further comprising;

a circuit,

wherein in said operation in response to said read command, said circuit senses status of data according to threshold voltage of said nonvolatile memory cell which is within whether said threshold voltage range indicating said erase state or said threshold voltage range indicating said program state.

14. A nonvolatile memory apparatus according to claim 10, wherein each of said nonvolatile memory cells has a threshold voltage within an arbitrary one of a plurality of threshold voltage ranges,

wherein said threshold voltage ranges include a threshold voltage range indicating an erase state and a plurality of threshold voltage ranges each indicating a corresponding program state, and

wherein said nonvolatile memory apparatus controls moving said threshold voltage of one said nonvolatile memory cell to within said threshold voltage ranges indicating said program states according to data and staying said threshold voltages of remaining memory cells of ones of said nonvolatile memory cells, in said operation in response to said program command.

15. A nonvolatile memory apparatus according to claim 14, wherein said commands further include an erase command,

wherein in an operation in response to said erase command received from said command terminal, said nonvolatile memory apparatus erases data stored in ones of said nonvolatile memory cells, and

wherein said nonvolatile memory apparatus controls moving said threshold voltages of ones of said nonvolatile memory cells to within said threshold voltage range indicating said erase state in said operation in

response to said erase command.